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EXAMINER	
ARCOS, CAROLINE H	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/733,174	OKA ET AL.	
	Examiner	Art Unit	
	CAROLINE ARCOS	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/11/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. JP2002-363780.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08/25/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-11 are pending for examination.

Specification

2. The abstract of the disclosure is objected to because all the numbers (e.g., 103A) this reference to figures in the abstract is improper. Correction is required. See MPEP § 608.01(b).

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.
   a. The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.
   b. The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1- 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

   a. The claim language in the following claims is not clearly understood:

      i. As per claim 1, lines 5-6 it is unclear what is meant by "operating environment (i.e. different modes or different workload?)

ii. As per claim 3, lines 1-3, it is unclear what are the criteria for selectively connect the external device to one of the component- processors or the component- processors to each other.

iii. As per claim 4, it has the same deficiency as claim 3.

iv. As per claim 7, it has same deficiency as claim 1.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Macias et al. (US 5,886,537), in view of Arnold et al. (US 5,175,837).

7. As per claim 1, Macias teaches the invention substantially as claimed including a signal processing device, comprising:

a general-purpose signal processor formed of an assembly of plural component-processors, each of the component-processors being capable of operating under operating environments independent of other component-processors (abs., lines 1-3; col. 3, lines 16-24; col. 3, lines 32-42); and

being capable of arbitrarily changing the operating environments of each of the

component-processors in accordance with a demand for signal processing (col. 3, lines 16-24; col. 5, lines 2-20).

8. Macias doesn't explicitly teach a management processor being capable of arbitrarily changing the operating environments of each of the component-processors in accordance with a demand for signal processing. However, Arnold teaches a management processor being capable of arbitrarily changing the operating environments of each of the component-processors in accordance with a demand for signal processing (col. 5, lines 45-65; col. 6, lines 58-63).

9. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Macias and Arnold because Arnold teaching of a management processor being capable of arbitrarily changing the operating environments of each of the component-processors in accordance with a demand for signal processing would improve Macias system performance by having a management processor that facilitate the communication in the system and regulate demand for signal processing of each of the component processors.

10. As per claim 2, Macias teaches swap one of the component-processors which receives the signal to be processed which is inputted through the input/output interface or outputs the processed signal in accordance with a demand for signal processing (abs., lines 1-3; col. 3, lines 16-24; col. 3, lines 32-42; col. 5, lines 2-20).

an input/output interface for receiving a signal to be processed inputted from an external device or one of the component-processors, and for outputting a processed signal to the external

device or one of the component-processors (fig. 1; col. 3, lines 31-52),

11. Macias doesn't explicitly teach that the management processor controls the input/output interface. However, Arnold teaches the management processor controls the input/output interface (col. 5, lines 45-65; col. 6, lines 58-63).

12. As per claim 3, Macias teaches that the input/output interface includes a cross bus switch that can selectively connect the external device to one of the component-processors, or the component-processors to each other (fig. 1).

13. As per claim 6, Arnold teaches the case including a first connection interface being connectable to a device that provides a demand for signal processing to the management processor, and a second connection interface being connectable to the external device that delivers a signal with respect to the input/output interface (fig. 1, 18, 20A).

14. The combined teaching of Macias and Arnold doesn't explicitly teach that the general-purpose signal processor, the management processor and the input/output interface are disposed in a single case. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to conclude form the combined teaching of Macias and Arnold that the processors exist in one system; it will be well known in the art to enclose the system in a single case which facilitate portability.

15. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Macias et al. (US 5,886,537), in view of Arnold et al. (US 5,175,837) as applied to claim 2 above and further in view of Iwase et al (US. 5,926,583).

16. As per claim 4, the combined teaching of Macias and Arnold doesn't explicitly teach that the input/output interface includes a multiple bus that can selectively connect the external device to one of the component-processors, or the component-processors to each other (Macias: fig. 1; col. 5, lines 30-37).

17. However, Iwase teaches that the input/output interface includes a multiple bus that can selectively connect the external device to one of the component-processors, or the component-processors to each other (col. 31, lines 20-32).

18. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Macias, Arnold and Iwase because Iwase teaching of selectively connect the external device to one of the component-processors, or the component-processors to each other would improve system performance and communication efficiency by regulating the connection between the component-processors.

19. As per claim 5, the combined teaching of Macias and Arnold doesn't explicitly teach that a local memory is disposed on each of the component-processors,

said local memory stores a signal to be processed or a signal processed result by the

component-processors until the signal to be processed or the signal processed result becomes available to be outputted to the input/output interface.

20. However, Iwase teaches that a local memory is disposed on each of the component-processors,

said local memory stores a signal to be processed or a signal processed result by the component-processors until the signal to be processed or the signal processed result becomes available to be outputted to the input/output interface (col. 31, lines 33-45).

21. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Macias, Arnold and Iwase because Iwase teaching of having local memory on each of the component-processor and said local memory stores a signal to be processed or a signal processed result by the component-processors until the signal to be processed or the signal processed result becomes available to be outputted to the input/output interface would improve system performance and efficiency in processing demand signal by storing the result in the memory to be retrieved whenever needed.

22. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Macias et al. (US 5,886,537), in view of McNeill et al. (US 4, 876, 643).

23. As per claim 7, Macias teaches an entertainment device, comprising:

a signal processing device including a general-purpose signal processor, and

management processor and an input/output interface (col. 3, lines 32-42; fig. 1; fig. 3);

wherein said general-purpose signal processor is formed of an assembly of plural component-processors (Abs., lines 1-3; col. 3, lines 17-25),

wherein each of the component-processors can operate in parallel under operating environments independent of other component-processors (abs., lines 1-3; col. 3, lines 16-24; col. 3, lines 32-42);

wherein the input/output interface inputs a signal to be processed from an external device or one of the component-processors, and outputs a processed signal to the external device or one of the component-processors(col. 3, lines 17-25; col. 3,lines 53-63; col. 5, lines 30-38; fig. 1; col. 3, lines 31-52).

swap one of the component-processors which receives the signal to be processed which is inputted through the input/output interface or outputs the processed signal in accordance with the demand for signal processing(abs., lines 1-3; col. 3, lines 16-24; col. 3, lines 32-42; col. 5, lines 2-20).

24. Macias doesn't explicitly teach that a signal processing device including a management processor and a main processor that provides a demand for signal processing to the signal processing device,

wherein the management processor sets the operating environments of each of the component-processors in accordance with a demand for signal processing which is provided from the main processor, and controls the input/output interface.

25. However, McNeill teaches a signal processing device including a management processor and a main processor that provides a demand for signal processing to the signal processing device (abs., lines 3-9; fig. 2, 210 and 212; col. 3, lines 50-59)

wherein the management processor sets the operating environments of each of the component-processors in accordance with a demand for signal processing which is provided from the main processor, and controls the input/output interface (fig. 2, 212; col. 10, lines 5-30).

26. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Macias and McNeill because McNeill teaching of management processor that sets the environment for the component- processor based on the signal received from the main processor would improve Macias system performance and efficiency by creating a hierarchy of commands and roles for every processor which facilitate the communication between the processors.

27. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Macias et al. (US 5,886,537), in view of McNeill et al. (US 4, 876, 643) as applied to claim 7 above and further in view of Row et al. (US 2002/0083111 A1).

28. As per claim 8, the combined teaching of Macias and McNeill doesn't explicitly teach that a network interface that enables a connection with a computer network, and a storage means that stores digital information readable by a computer,

wherein the main processor controls the network interface to acquire the digital

information from an external device, stores the acquired digital information in the storage means, and provides the stored digital information and a demand for signal processing based on the digital information to the management processor of the signal processing device to constitute operating environments for entertainment processing the contents of which are determined in accordance with the digital information.

29. However, Row teaches a network interface that enables a connection with a computer network, and a storage means that stores digital information readable by a computer, wherein the main processor controls the network interface to acquire the digital information from an external device, stores the acquired digital information in the storage means, and provides the stored digital information and a demand for signal processing based on the digital information to the management processor of the signal processing device to constitute operating environments for processing the contents of which are determined in accordance with the digital information (fig. 2; claim 1).

30. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Macias, McNeill and Row because Row teaching of network interface controlled by the main processor would improve system compatibility and efficiency and expand its usage over the network.

31. The combined teaching of Macias, McNeill and Row doesn't explicitly teach that the operating environments for entertainment processing. However, it would have been obvious 6to

one of ordinary skill in the art at the time the invention was made to make use of the combined teaching of Macias, McNeill and Row in any field in the industry including entertainment processing.

32. As per claim 9, McNeill teaches the main processor constructs the operating environments for entertainment processing on one or more of the component-processors through the management processor, and, after constructing the operating environments,

said main processor reconstructs said operating environments to new operating environments upon receipt of another digital information which differs from said digital information (col. 3, lines 50-60; col. 4, lines 35-53).

33. Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Macias et al. (US 5,886,537), in view of McNeill et al. (US 4, 876, 643) , in view of Row et al. (US 2002/0083111 A1) , in view of Row et al. (US 2002/0083111 A1) as applied to claim 8 above and further in view of Gorgone et al. (US 2003/0200249 A1).

34. As per claim 10, The combined teaching of Macias, McNeill and Row doesn't explicitly teach that the digital information comprises plural kinds of application programs that can execute required functions, respectively, and

wherein the management processor assigns any of the functions to the corresponding component-processors, and reads the application program for executing the assigned function from the storage means, and executes the application program.

35. However, Gorgone teaches plural kinds of application programs that can execute required functions, respectively, and

wherein the management processor assigns any of the functions to the corresponding component-processors, and reads the application program for executing the assigned function from the storage means, and executes the application program (Par. [0016]).

36. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Macias, McNeill , Row and Gorgone because Gorgone teaching of processing plurality of application kinds with different function would improve the performance and efficiency and the diversity of processing application and increase the throughput.

37. As per claim 11, Mcneill teaches that each of the component-processors operates only for executing the application program for executing the function assigned to the component-processor until the management processor provides another demand to the component-processor (abs., lines 3-9; col. 3, lines 50-60).

Conclusion

38. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US 5491787 A teach Fault tolerant digital computer system having two processors which periodically alternate as master and slave.

US 6910085 B2 teach Audio visual system having a serial bus for identifying devices connected

to the external terminals of an amplifier in the system.

US 6119217 A teach Information processing apparatus and information processing method.

US 5657449 A teach Exchange control system using a multiprocessor for setting a line in response to line setting data.

US 5522083 A teach Reconfigurable multi-processor operating in SIMD mode with one processor fetching instructions for use by remaining processors.

US 5392391 A teaches High performance graphics applications controller.

39. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CAROLINE ARCOS whose telephone number is (571)270-3151. The examiner can normally be reached on Monday-Thursday 7:00 AM to 5:30 PM.

40. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

41. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would

like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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